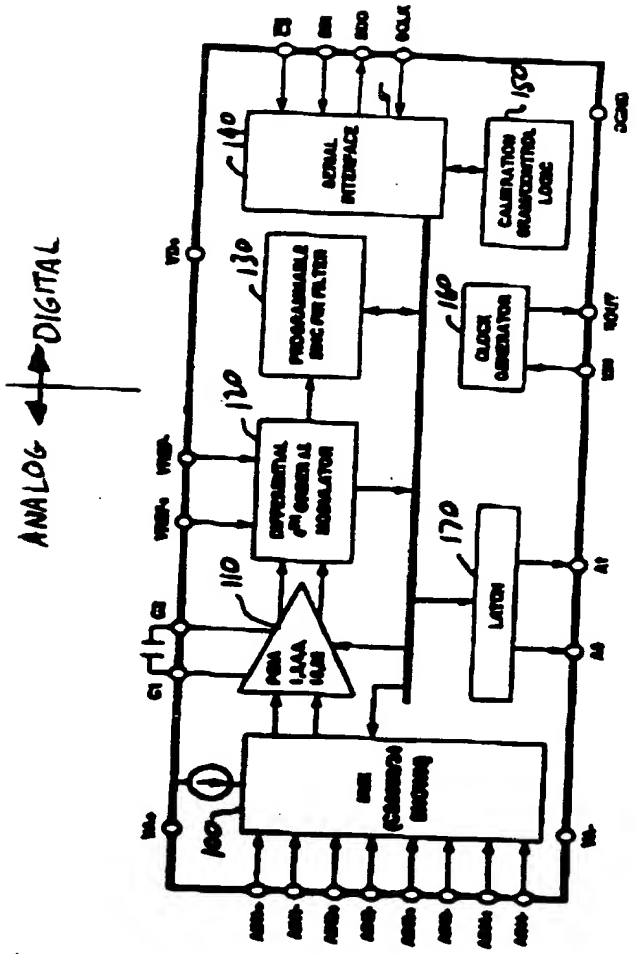

ANALOG
DIGITAL
110
120
130
140
150
160
170
SERIAL INTERFACE
CALIBRATION MANIPULATION LOGIC
PROGRAMMABLE SINC FIR FILTER
CLOCK GENERATOR
LATCH

FIGURE 1.1A

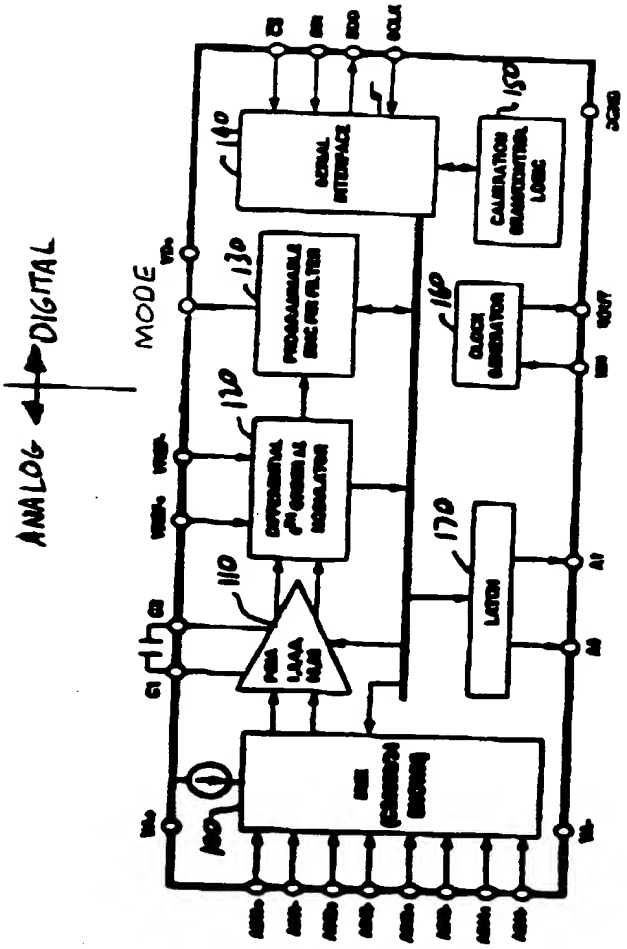

ANALOG
DIGITAL
MODE
110
120
130
140
150
160
170
180
SERIAL INTERFACE
CALIBRATION REGISTER/CONTROL LOGIC
PROGRAMMABLE DECIMATION FILTER
CLOCK GENERATOR
DIFFERENTIAL ΔΣ MODULATOR
LATCH
BIAS GENERATOR

FIGURE 1.1B

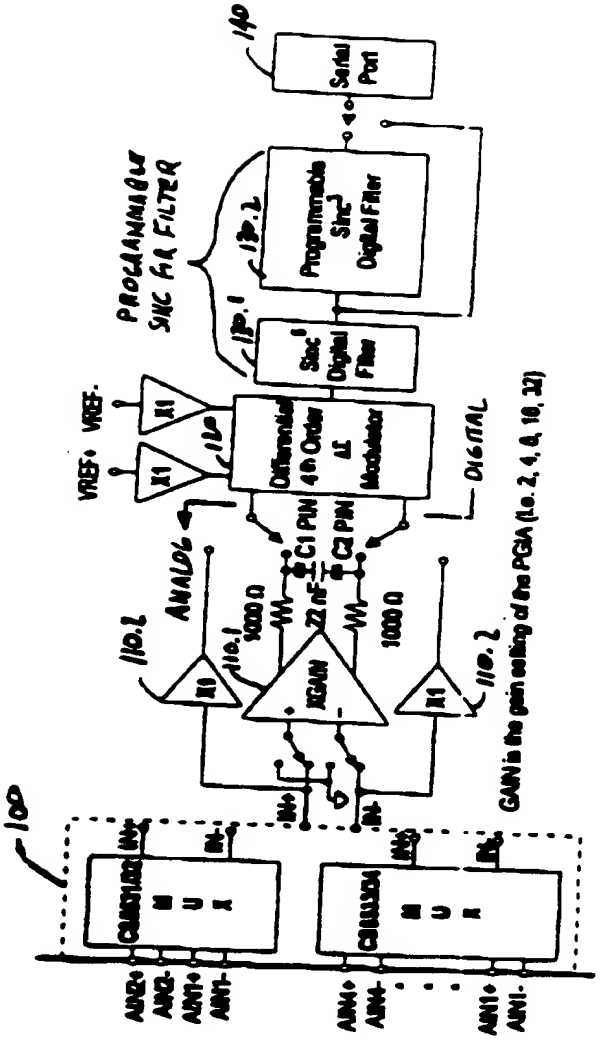


FIGURE 1.2A

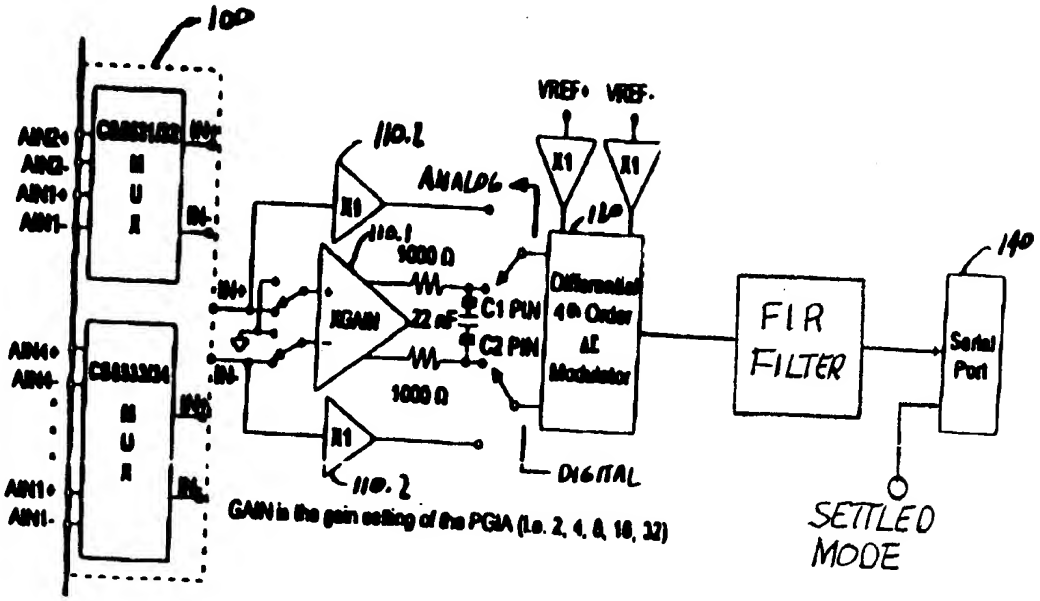


FIGURE 1.2 B

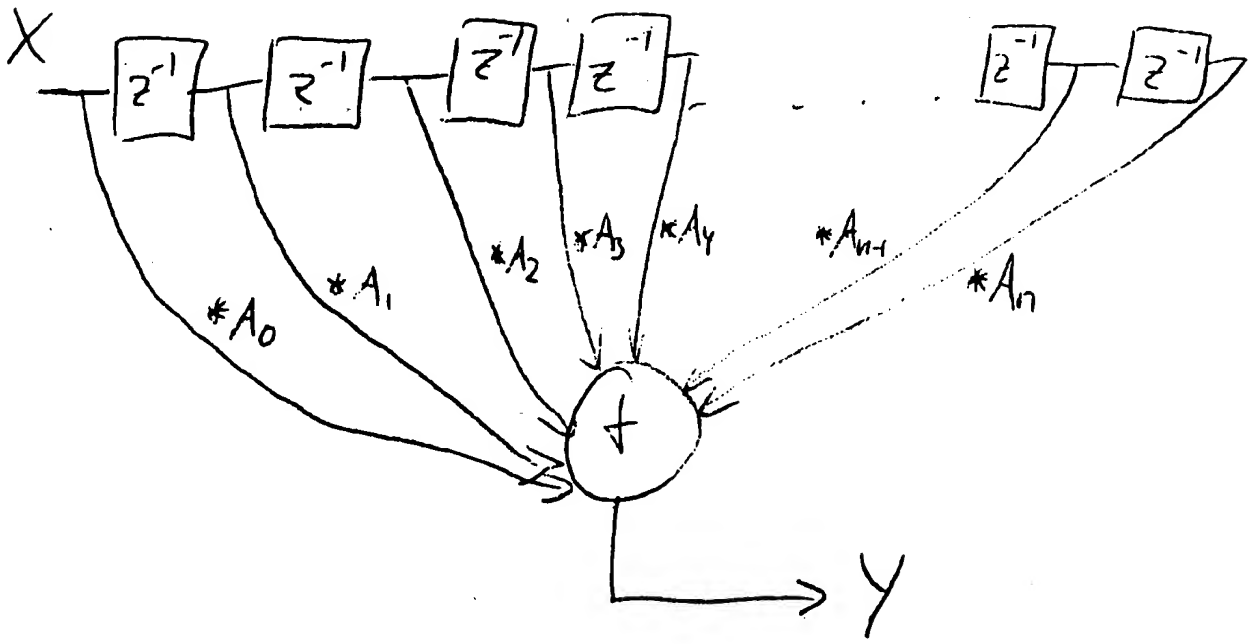


FIG 1.2C

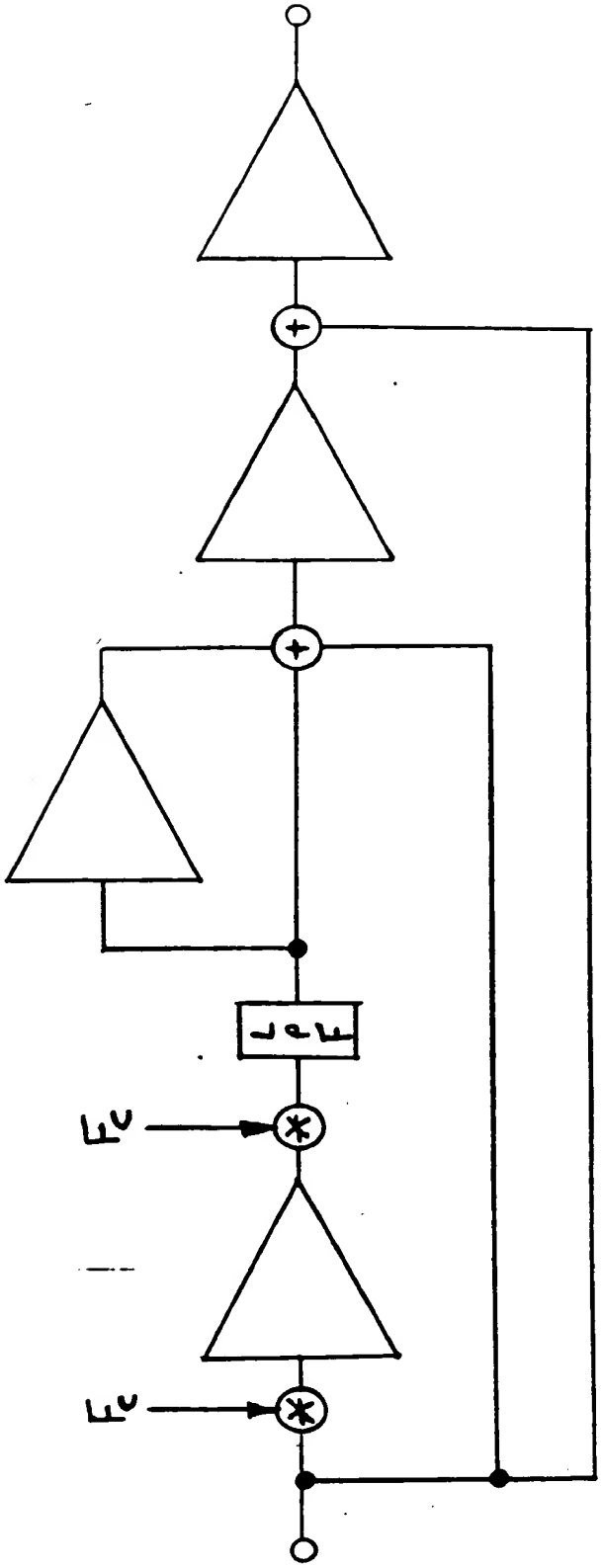


FIGURE 1.3

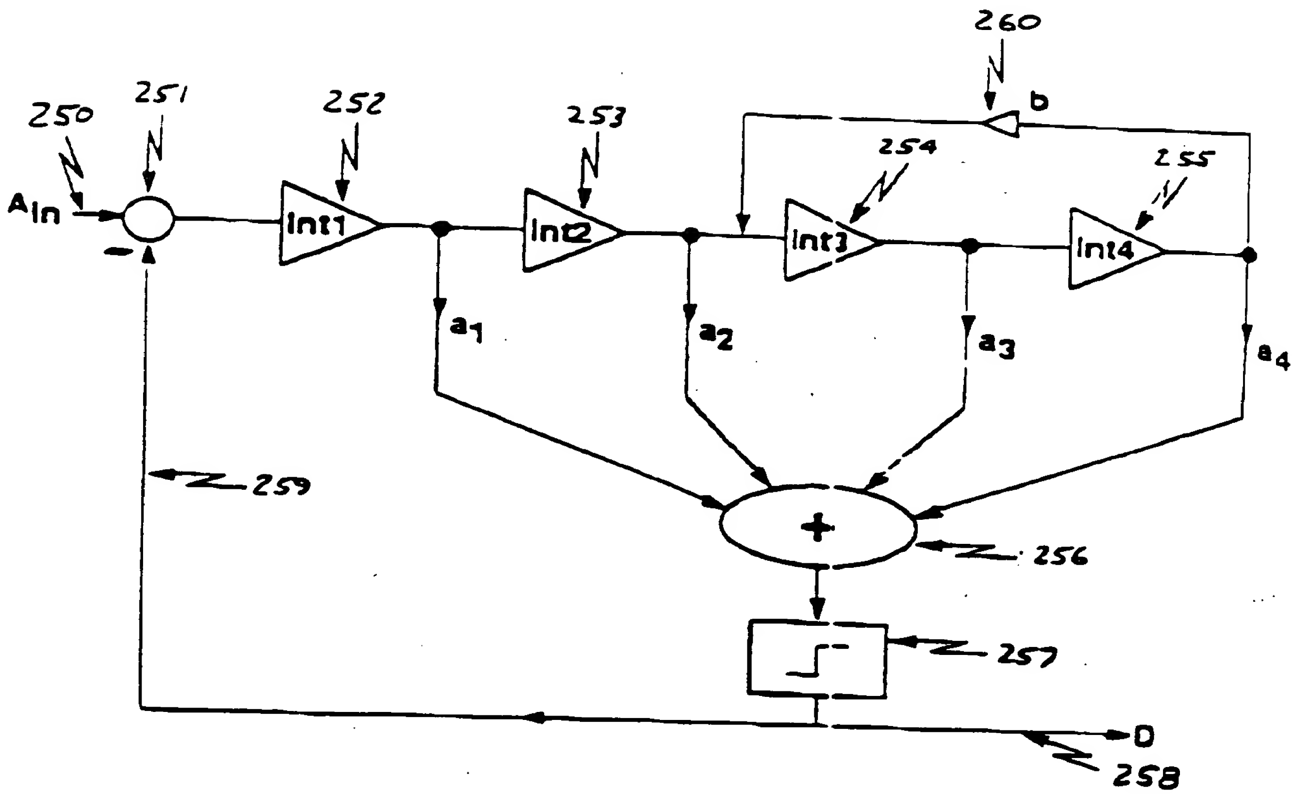


Figure 1.4

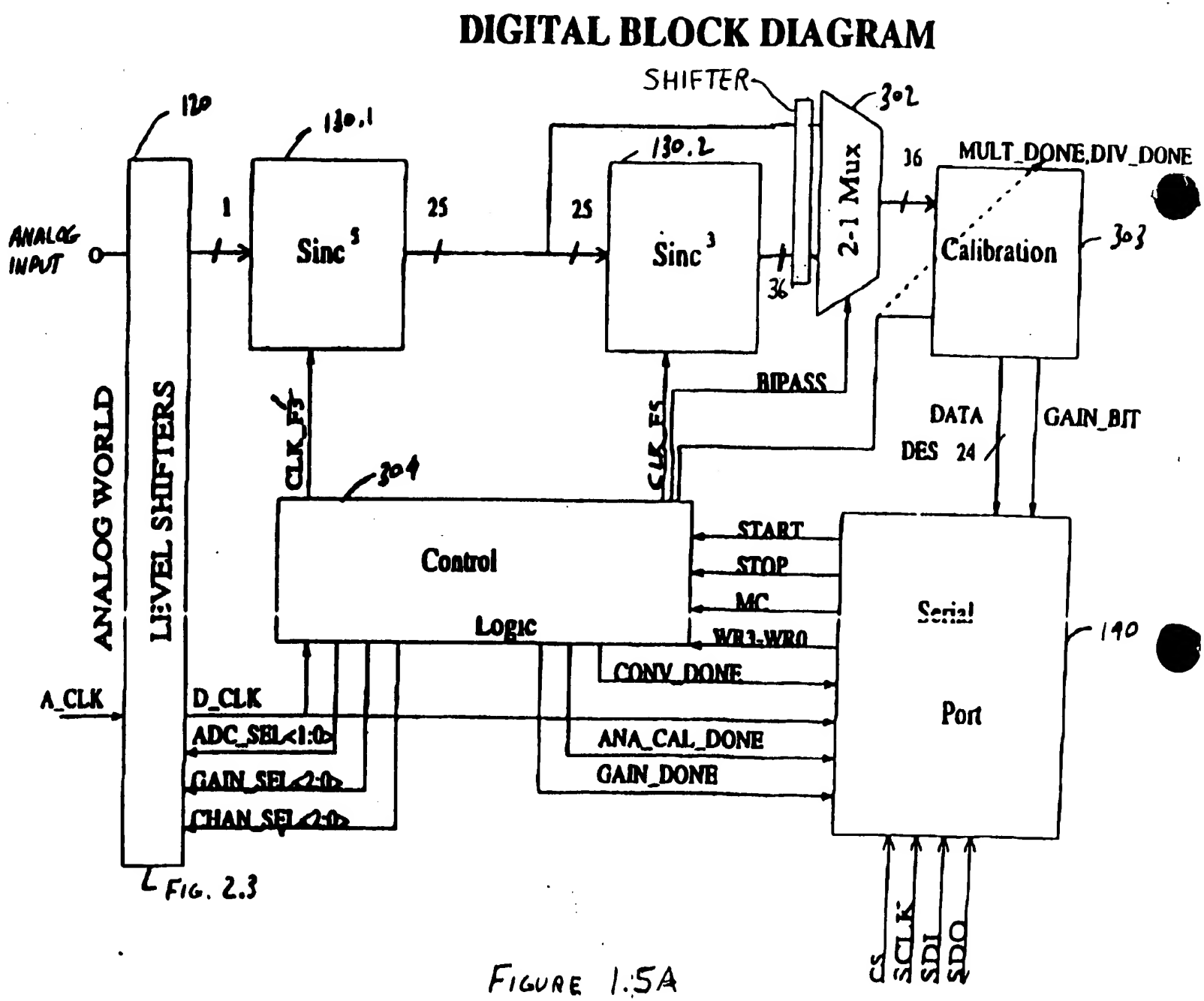


FIG. 2.3

FIGURE 1.5A

DIGITAL BLOCK DIAGRAM

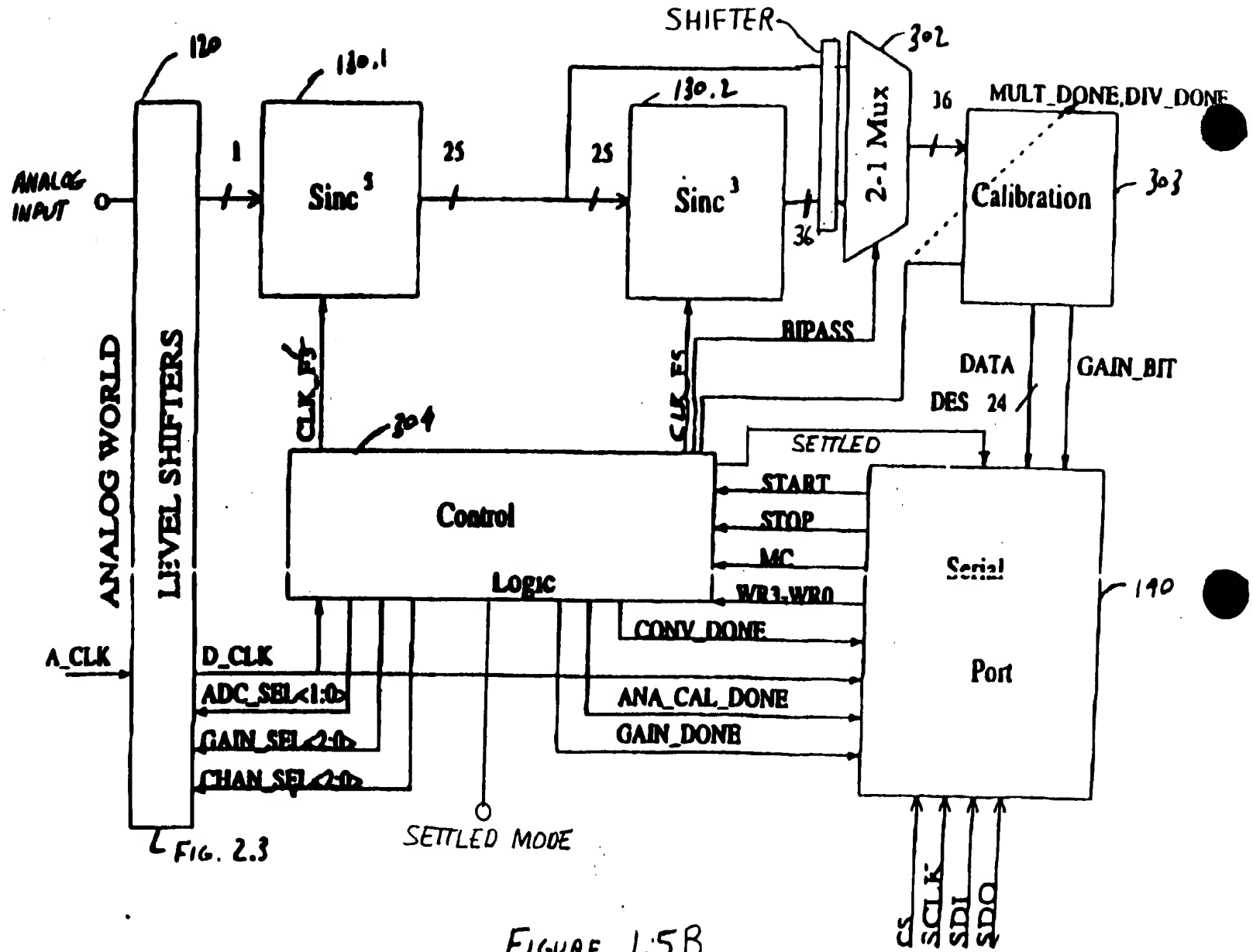


FIG. 2.3

FIGURE 1.5B

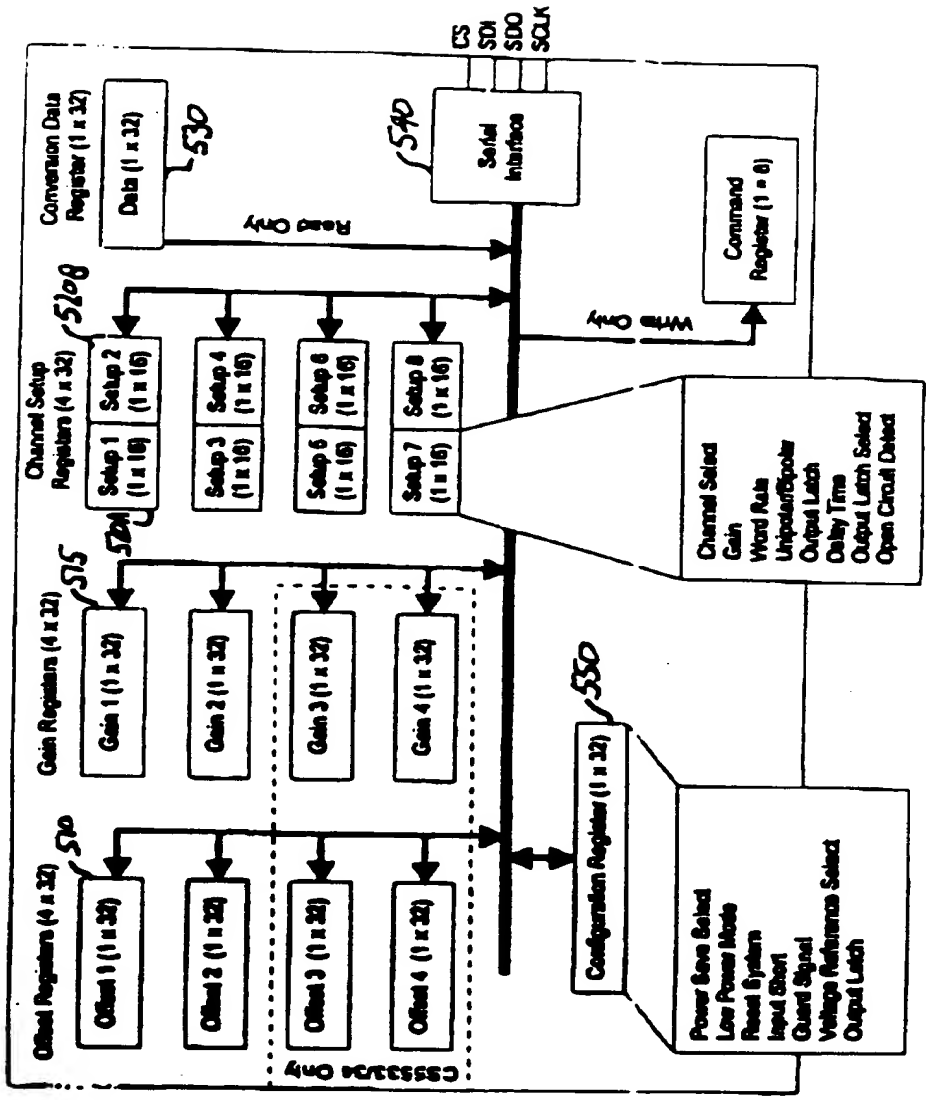

CS
SDI
SDO
SCLK
Conversion Data Register (1 x 32)
Data (1 x 32)
530
Read Only
540
Serial Interface
Command Register (1 x 8)
Write Only
Channel Setup Registers (4 x 32)
510
Setup 1 (1 x 16)
Setup 2 (1 x 16)
Setup 3 (1 x 16)
Setup 4 (1 x 16)
Setup 5 (1 x 16)
Setup 6 (1 x 16)
Setup 7 (1 x 16)
Setup 8 (1 x 16)
520
Channel Select
Gain
Word Rate
Unipolar/Bipolar
Output Latch
Delay Time
Output Latch Select
Open Circuit Detect
Gain Registers (4 x 32)
515
Gain 1 (1 x 32)
Gain 2 (1 x 32)
Gain 3 (1 x 32)
Gain 4 (1 x 32)
Offset Registers (4 x 32)
505
Offset 1 (1 x 32)
Offset 2 (1 x 32)
Offset 3 (1 x 32)
Offset 4 (1 x 32)
550
Configuration Register (1 x 32)
Power Save Select
Low Power Mode
Reset System
Input Short
Guard Signal
Voltage Reference Select
Output Latch
AIO Processor

FIGURE 1.6A

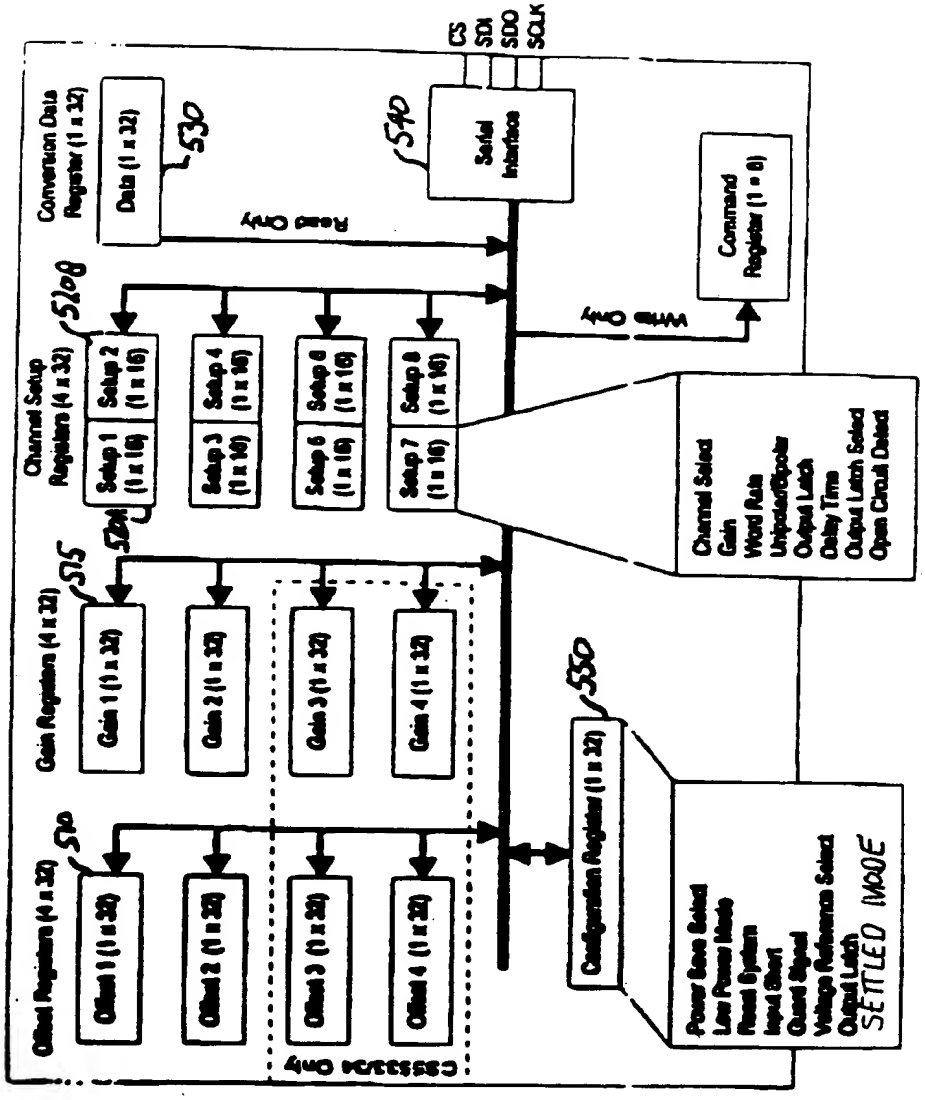

CS
SDI
SDO
SCLK
Conversion Data Register (1 x 32)
Data (1 x 32)
530
Read Only
540
Serial Interface
Command Register (1 x 8)
Write Only
Channel Setup Registers (4 x 32)
520B
Setup 1 (1 x 16)
Setup 2 (1 x 16)
Setup 3 (1 x 16)
Setup 4 (1 x 16)
Setup 5 (1 x 16)
Setup 6 (1 x 16)
Setup 7 (1 x 16)
Setup 8 (1 x 16)
520A
Channel Select
Gain
Word Rate
Unipolar/Bipolar
Output Latch
Delay Time
Output Latch Select
Open Circuit Detect
515
Gain Registers (4 x 32)
Gain 1 (1 x 32)
Gain 2 (1 x 32)
Gain 3 (1 x 32)
Gain 4 (1 x 32)
550
Configuration Register (1 x 32)
510
Offset Registers (4 x 32)
Offset 1 (1 x 32)
Offset 2 (1 x 32)
Offset 3 (1 x 32)
Offset 4 (1 x 32)
Power Save Select
Low Power Mode
Reset System
Input Short
Guard Signal
Voltage Reference Select
Output Latch
SETTLED MODE
Calibration Only

FIGURE 1.6B

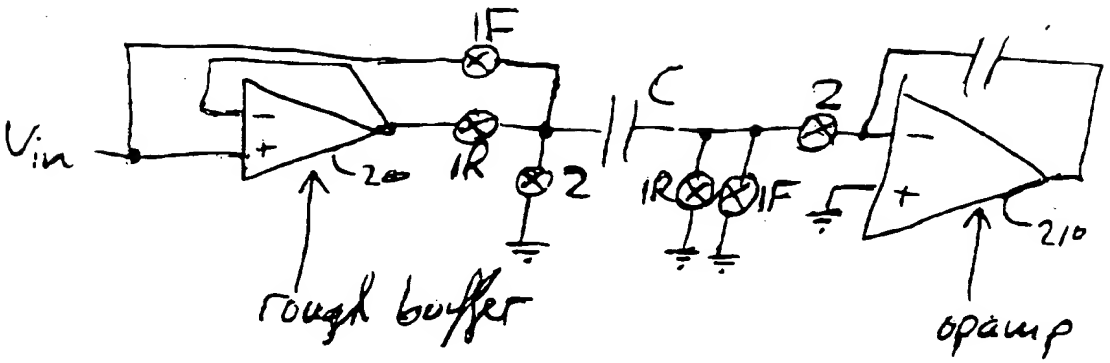


FIGURE 2.0

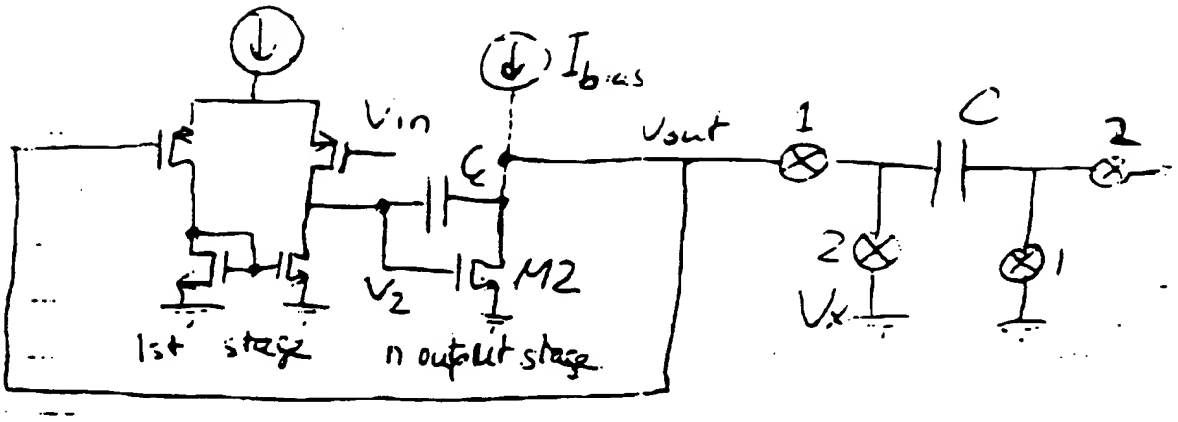


FIGURE 2.1

V_{IN} = CONSTANT

$V_{OUT} > V_X$

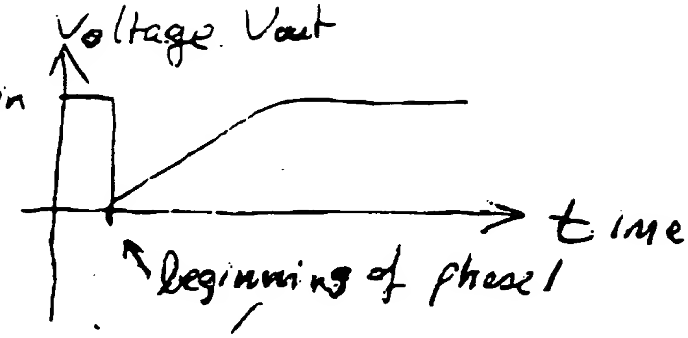


FIGURE 2.2

V_{IN} = CONSTANT

$V_{OUT} < V_X$

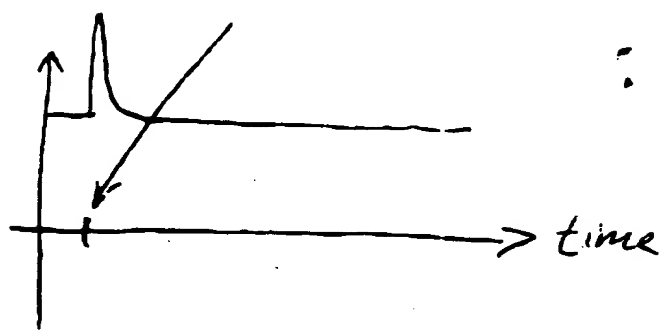


FIGURE 2.3

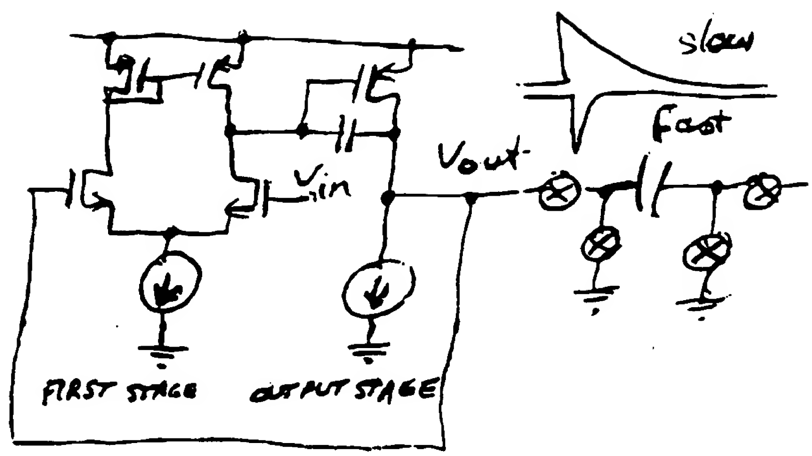


FIGURE 2.4

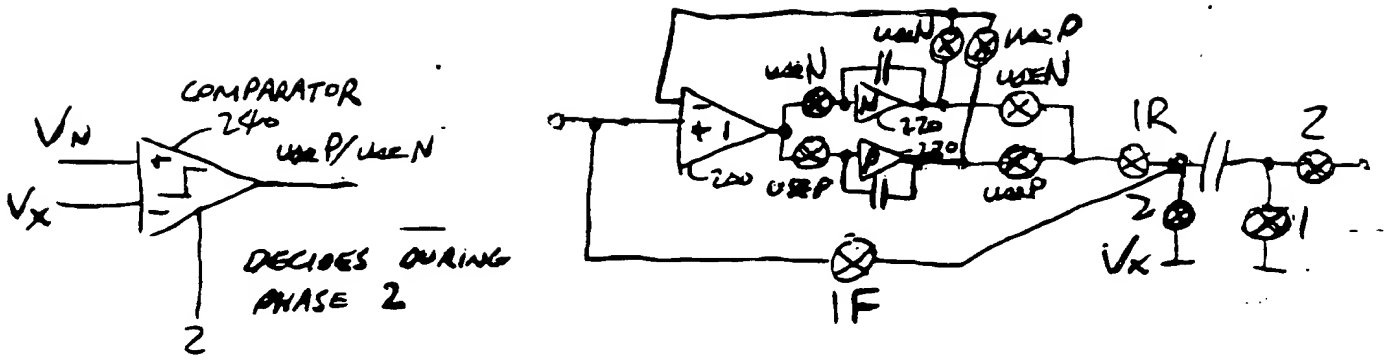
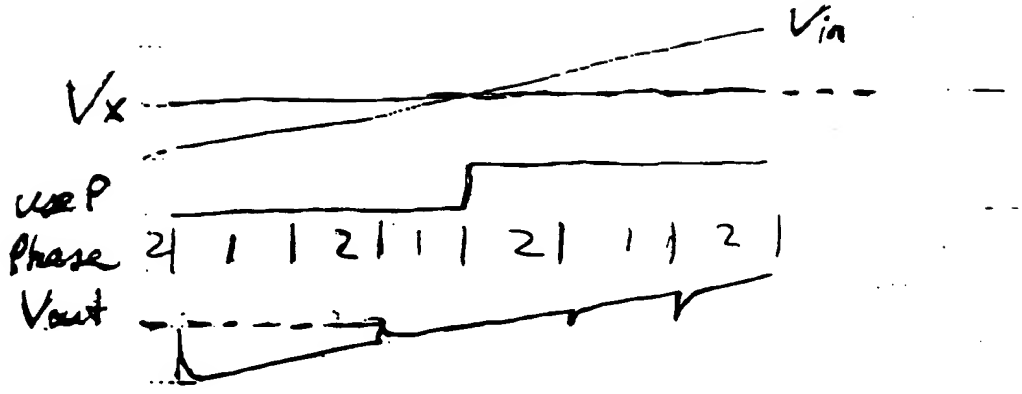


FIGURE 2.5

FIGURE 2.6

FIGURE 2.7

FIGURE 2.8



MULTIPLIER ARCHITECTURE

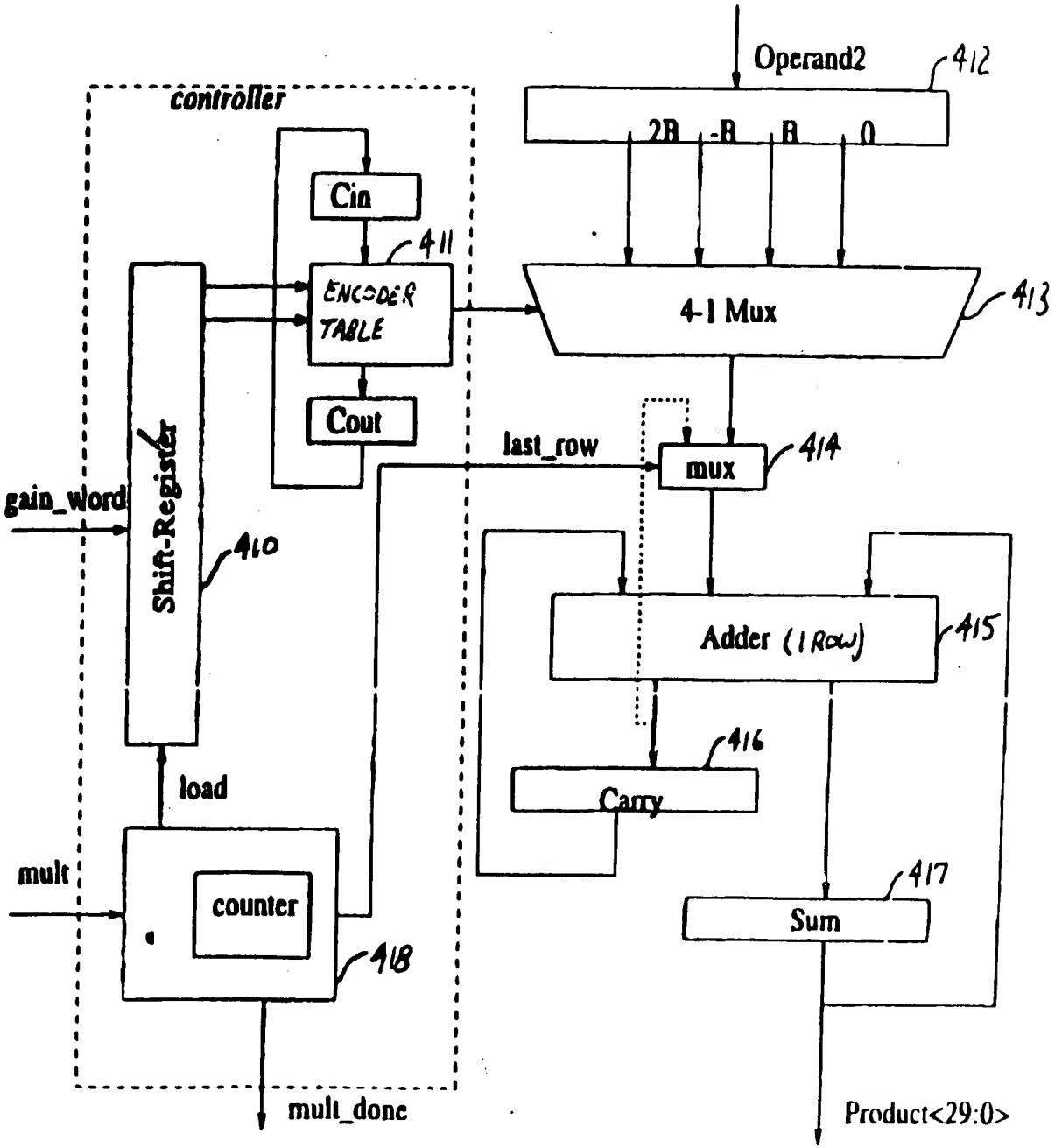


FIGURE 3.1

Multiplication

FIGURE 3.2
(PRIOR ART)

Table 2: Encoding Scheme Proposed

A_{i+1}	A_i	Operation
0	0	$R_i = R_{i-1}/4$
0	1	$R_i = (R_{i-1} + B)/4$
1	0	$R_i = (R_{i-1} + 2B)/4$
1	1	$R_i = (R_{i-1} + 3B)/4$

FIGURE 3.3
(PRIOR ART)

Table 3: Carry Propagate Encoding Scheme

C_{in}	A_{i+1}	A_i	Operation	C_{out}
0	0	0	$R_i = R_{i-1}/4$	0
0	0	1	$R_i = (R_{i-1} + B)/4$	0
0	1	0	$R_i = (R_{i-1} + 2B)/4$	0
0	1	1	$R_i = (R_{i-1} - B)/4$	1
1	0	0	$R_i = (R_{i-1} + B)/4$	0
1	0	1	$R_i = (R_{i-1} + 2B)/4$	0
1	1	0	$R_i = (R_{i-1} - B)/4$	0
1	1	1	$R_i = (R_{i-1})/4$	1

Multiplication

FIGURE 3.4

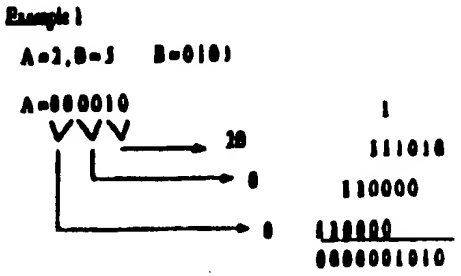
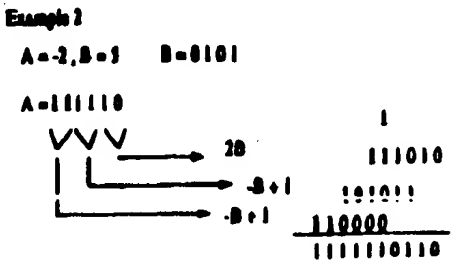


FIGURE 3.5



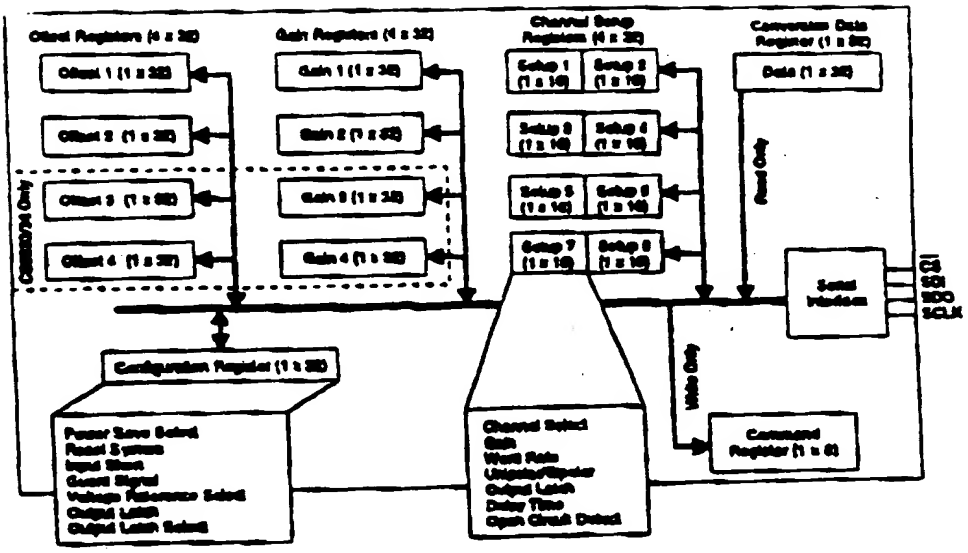


FIGURE 4.1

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
0	ARA	CS1	CS0	R/$\overline{W}$	RSB2	RSB1	RSB0

BIT	NAME	VALUE	FUNCTION
D7	Command Bit, C	0	Must be logic 0 for these commands.
		1	These commands are invalid if this bit is logic 1.
D6	Access Registers as Arrays, ARA	0	Ignore this function.
		1	Access the respective registers, offset, gain, or channel-setup, as an array of registers. The particular registers accessed are determined by the RS bits. The registers are accessed MSB first with physical channel 0 accessed first followed by physical channel 1 next and so forth.
D5-D4	Channel Select Bits, CS1-CS0	00	CS1-CS0 provide the address of one of the two (four for CS5533/34) physical input channels. These bits are also used to access the calibration registers associated with the respective physical input channel. Note that these bits are ignored when reading data register.
		01	
		10	
		11	
D3	Read/$\overline{\text{Write}}$, R/$\overline{W}$	0	Write to selected register.
		1	Read from selected register.
D2-D0	Register Select Bit, RSB3-RSB0	000	Reserved
		001	Offset Register
		010	Gain Register
		011	Configuration Register
		100	Conversion Data Register (Read Only)
		101	Channel-Setup Registers
		110	Reserved
		111	Reserved

FIGURE 4.2

D7(MSB)	D6	D5	D4	D3	D2	D1	D0
1	MC	CSRP2	CSRP1	CSRP0	CC2	CC1	CC0

BIT	NAME	VALUE	FUNCTION
D7	Command Bit, C	0	These commands are invalid if this bit is logic 0.
		1	Must be logic 1 for these commands.
D6	Multiple Conversions, MC	0	Perform fully settled single conversions.
		1	Perform conversions continuously.
D5-D3	Channel-Setup Register Pointer Bits, CSRP	000 ... 111	These bits are used as pointers to the Channel-Setup registers. Either a single conversion or continuous conversions are performed on the channel setup register pointed to by these bits.
D2-D0	Conversion/Calibration Bits, CC2-CC0	000	Normal Conversion
		001	Self-Offset Calibration
		010	Self-Gain Calibration
		011	Reserved
		100	Reserved
		101	System-Offset Calibration
		110	System-Gain Calibration
		111	Reserved

FIGURE 4.3

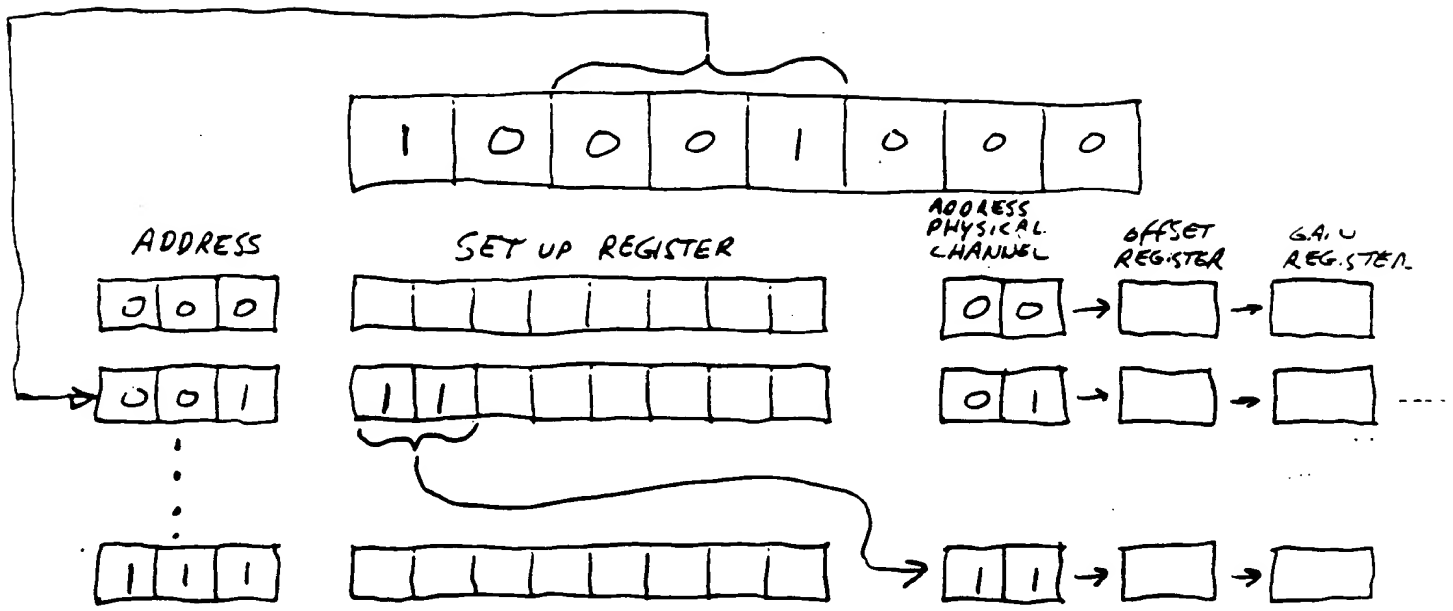

1 0 0 0 1 0 0 0
ADDRESS
SET UP REGISTER
ADDRESS PHYSICAL CHANNEL
OFFSET REGISTER
G.A.U REGISTER
0 0 0
0 0 1
1 1 1
0 0
0 1
1 1

FIGURE 4.4

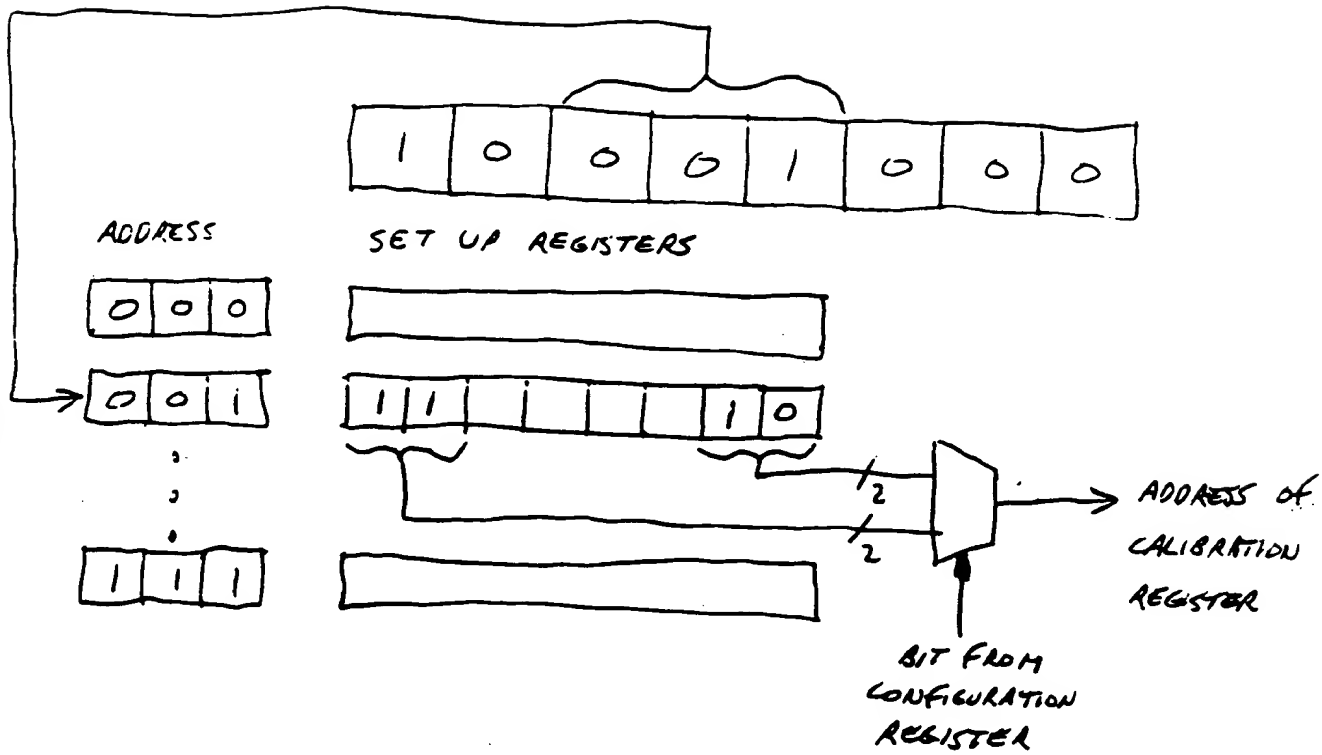

1 0 0 0 1 0 0 0
ADDRESS
SET UP REGISTERS
0 0 0
0 0 1
1 1
1 0
1 1 1
2
2
ADDRESS of CALIBRATION REGISTER
BIT FROM CONFIGURATION REGISTER

FIGURE 4.5

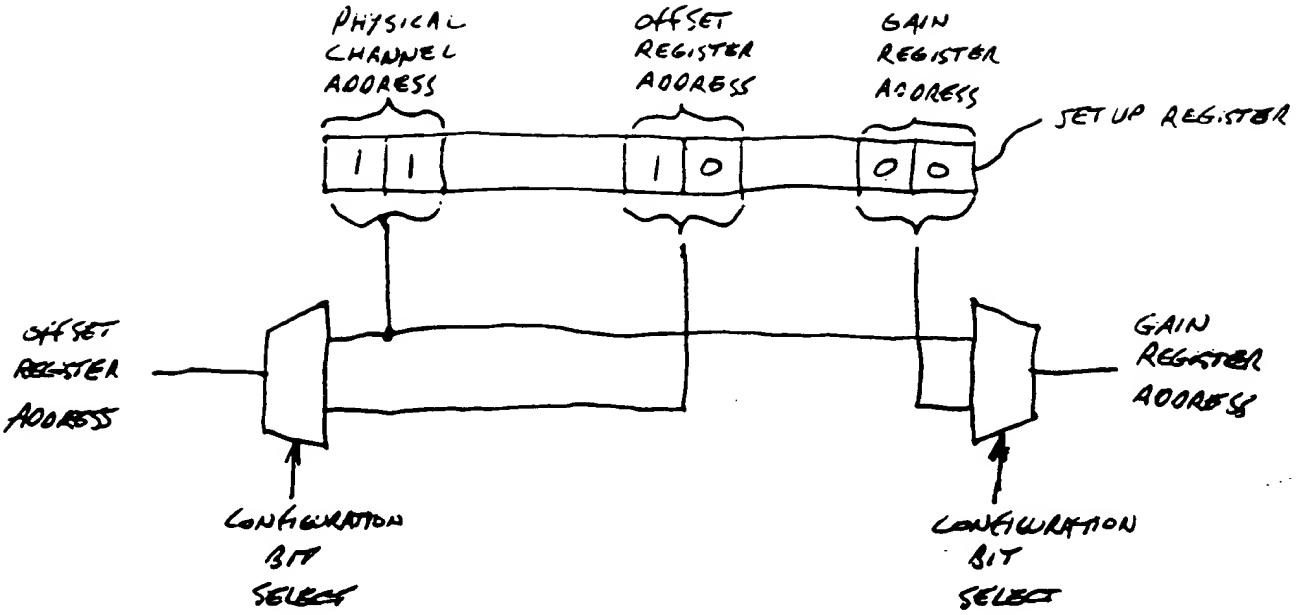

PHYSICAL CHANNEL ADDRESS
OFFSET REGISTER ADDRESS
GAIN REGISTER ADDRESS
SET UP REGISTER
1 1
1 0
0 0
OFFSET REGISTER ADDRESS
GAIN REGISTER ADDRESS
CONFIGURATION BIT SELECT
CONFIGURATION BIT SELECT

FIGURE 4.6

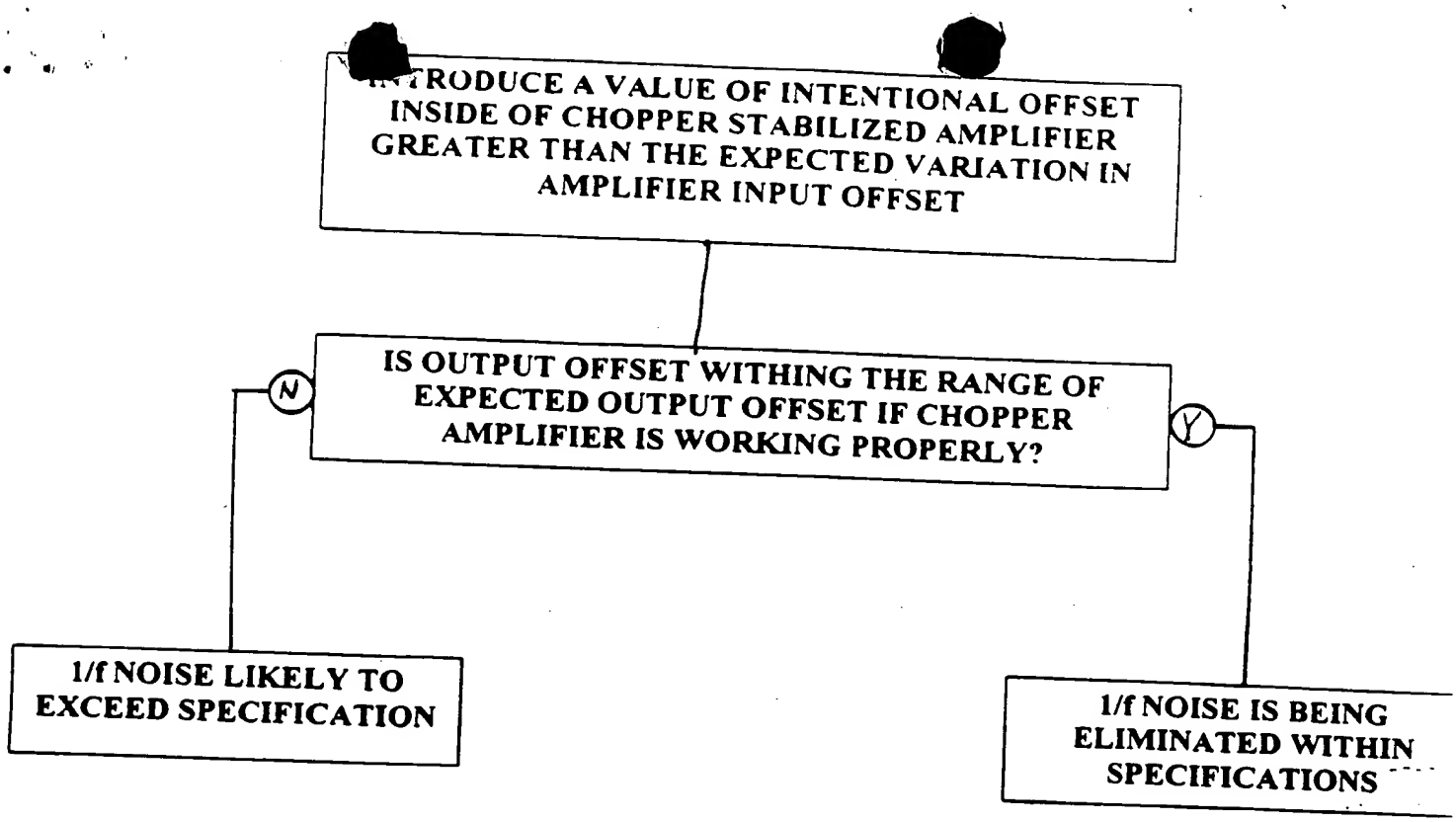

INTRODUCE A VALUE OF INTENTIONAL OFFSET INSIDE OF CHOPPER STABILIZED AMPLIFIER GREATER THAN THE EXPECTED VARIATION IN AMPLIFIER INPUT OFFSET
IS OUTPUT OFFSET WITHING THE RANGE OF EXPECTED OUTPUT OFFSET IF CHOPPER AMPLIFIER IS WORKING PROPERLY?
N
Y
1/f NOISE LIKELY TO EXCEED SPECIFICATION
1/f NOISE IS BEING ELIMINATED WITHIN SPECIFICATIONS

FIGURE 5.1

Thermocouple Application

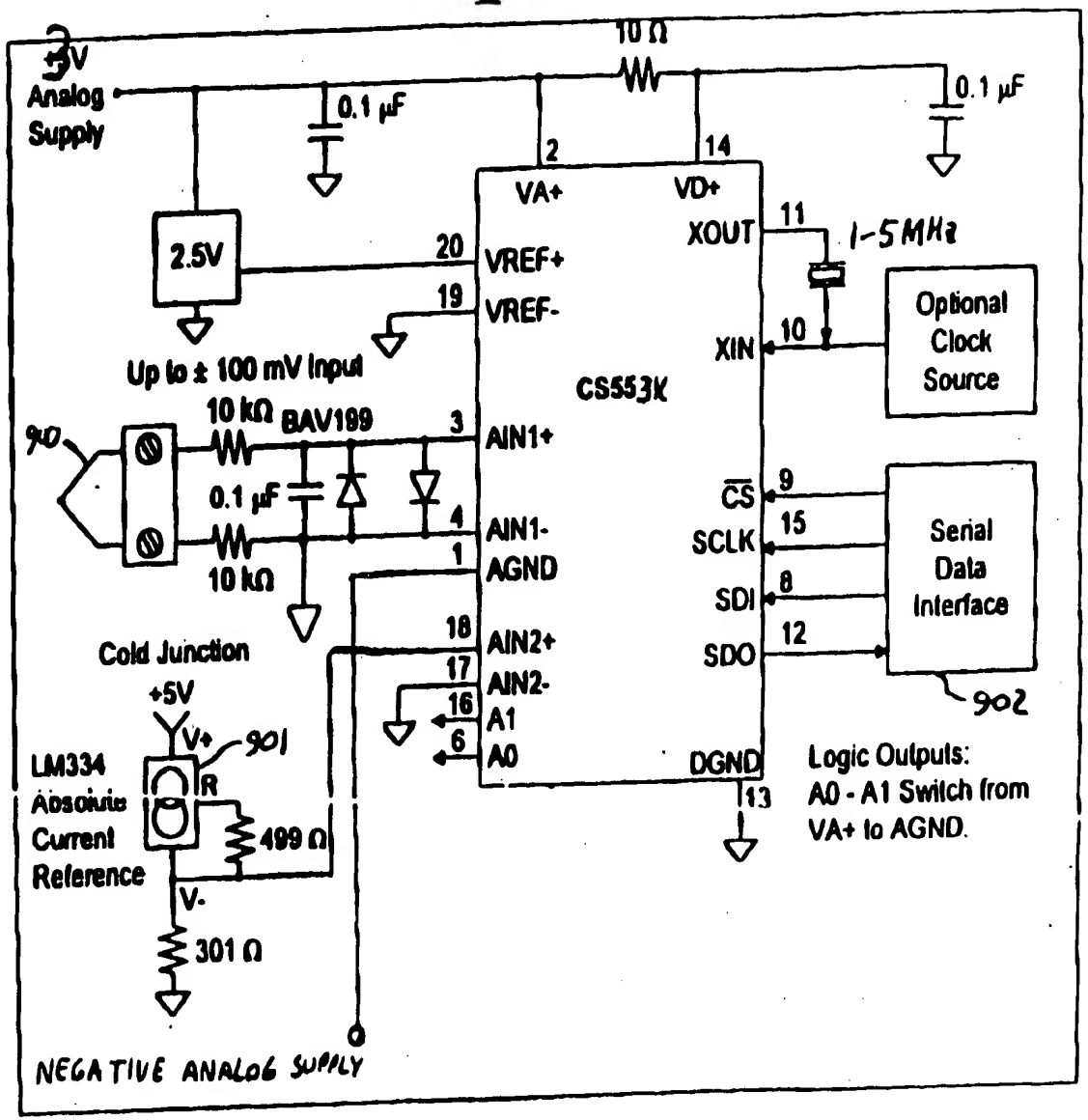


FIGURE 6.1

Bridge Transducer Application

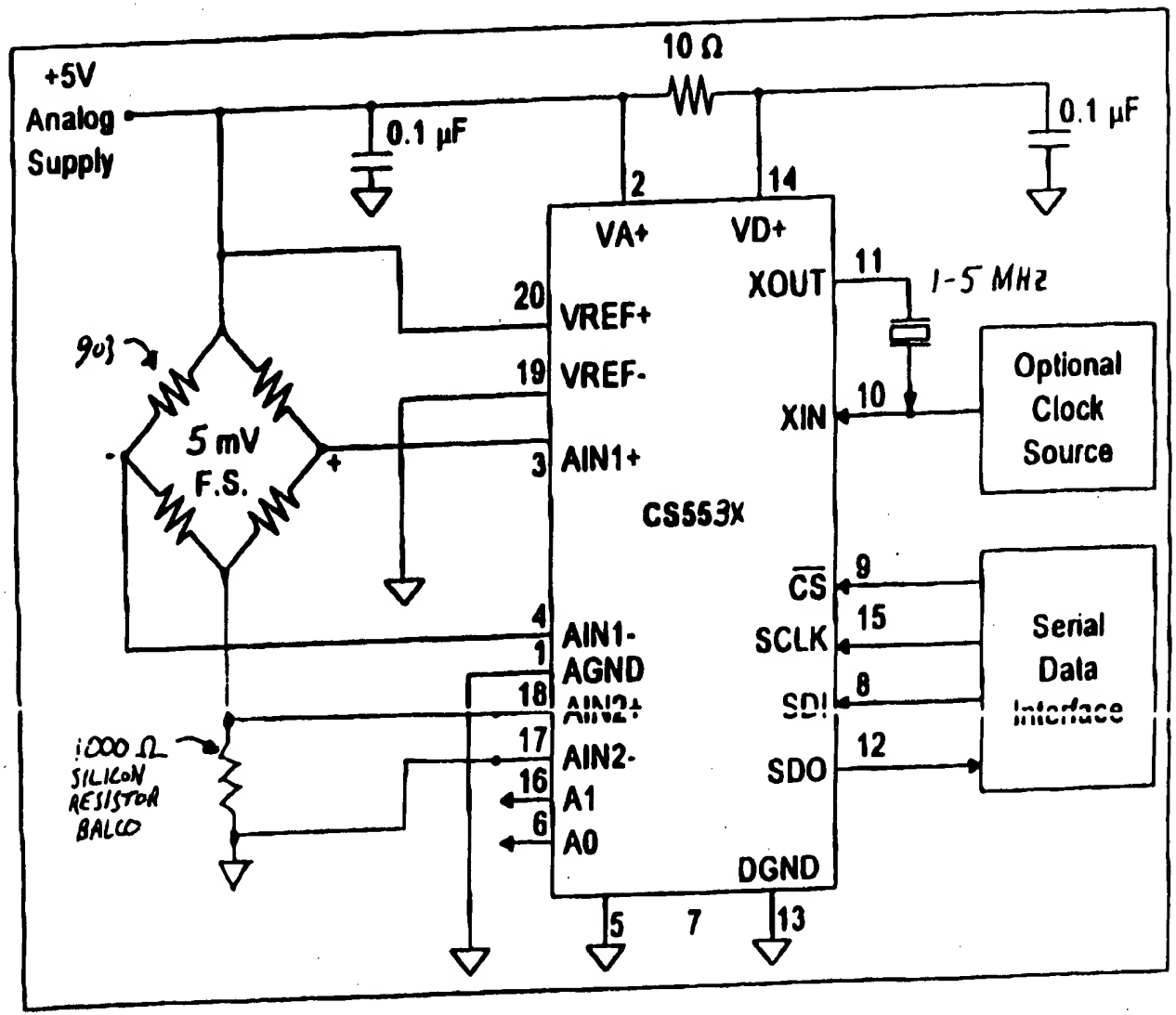


FIGURE 6.2